REMARKS

In the Office Action, the Examiner noted that claims 1-22 are pending in the application and that claims 1-22 are rejected. By this response, Applicants herein cancel claims 7-8, 12-14, and 18-22 and amend claims 1, 5-6, 9, 11, and 15-17. Claims 2-4 and 10 continue unamended. No new matter has been entered.

In view of both the amendments presented above and the following remarks, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, Applicants believe that all the claims are allowable.

It is to be understood that Applicants, by amending the claims, do not acquiesce to the Examiner's characterizations of the art of record or to Applicants' subject matter recited in the pending claims. Further, Applicants are not acquiescing to the Examiner's statements as to the applicability of the art of record to the pending claims by filing the instant responsive amendments.

Applicants' Representative thanks Examiner Anh-Vu Ly for the telephone conversation to discuss Applicants' case. Applicants' Representative is aware of the time constraints placed on the Examiner and appreciates the opportunity to bring the outstanding issues to quick resolution in this manner. During the discussion the Examiner indicated, based on a preliminary search of the prior art, that amendment of Applicants' claim 1 to include both a first input bit map and a second input bit map may result in claim 1 being allowable, although the Examiner did indicate that a full search may be required before a claim of such scope is allowed. Similarly, the Examiner indicated, based on a preliminary search of the prior art, that amendment of Applicants' other independent claims to include a first output bit map and a second output bit map (or, alternatively, a first input bit map and a second input bit map) may be allowable, although the Examiner did indicate that a full search may be required before claims of such scope are allowed. Applicants' Representative thanks the Examiner for taking the time to perform such a preliminary search and appreciate Examiner's efforts to indicate a claim scope that may be allowable over the prior art.

Objections

Claim 8

The Examiner has objected to claim 8 stating that "the first output bit map" lacks antecedent basis. In view of the fact that Applicants have herein cancelled claims 7-8 and amended claims 6 and 9 to clearly distinguish between the "first T2 X R2 output bit map" and the "second T2 X R2 output bit map", Applicants maintain that the objection should be withdrawn. Similarly, Applicants have herein cancelled claims 12-13 and amended claims 11 and 14 to clearly distinguish between the "first T2 X R2 input bit map" and the "second T2 X R2 input bit map". No new matter has been entered.

Rejections

35 U.S.C. § 102

The Examiner has rejected claims 1-22 under 35 U.S.C. §102 as being anticipated by Lindberg (U.S. Patent 6,366,579 B1, hereinafter "Lindberg"). The Applicants respectfully traverse the rejection.

In general, Lindberg discloses a modular time-space (TS) switch in which part of the space switch functionality of the TS switch core is arranged in groups of switch adapter boards and the TS switch core is divided into a matrix of independent TS-modules associated with the switch adapter boards. Specifically, Lindberg further discloses that each group of switch adapter boards cooperates with a predetermined row of the TS-modules in the matrix for input of data to TS-modules in that row, and with a predetermined column of the TS-modules in the matrix for output of data to TS-modules in that column. (Lindberg, Abstract).

Lindberg, however, does not teach or suggest each and every element of Applicants' invention as recited in independent claim 1 as amended. For example, Lindberg fails to teach or suggest at least the limitations of "at least one apparatus for conveying said selected bit pack to any output data position within a first output bit map including a combination of output data rails and time slots" and "at least one apparatus for loading a second output bit map including a combination of output data rails and time slots from said first output bit map, said second

output bit map configurable for being loaded in parallel with said first output bit map." Specifically, Applicants' invention of claim 1 positively recites:

> "Apparatus for switching data from any of a plurality of inputs to any of a plurality of outputs, comprising:
> at least one apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots and for storing said received bit packs in matrix form including a storage position for each rail and time slot combination;
> at least one apparatus for selecting any of the input bit packs from any of the rails in any of the time slots of said matrix;
> at least one apparatus for conveying said selected bit pack to any output data position within a first output bit map including a combination of output data rails and time slots; and
> at least one apparatus for loading a second output bit map including a combination of output data rails and time slots from said first output bit map, said second output bit map configurable for being loaded in parallel with said first output bit map."
> (Emphasis added.)

As evident from Applicants' disclosure and claims, Applicants' invention is directed, at least in part, to an apparatus for switching data from any of a plurality of inputs to any of a plurality of outputs. In particular, Applicants' invention of at least claim 1 teaches at least one apparatus for conveying bit packs selected from any of the rails in any of the time slots of a matrix to any output data position within a combination of output data rails and time slots. Furthermore, Applicants' invention of at least claim 1 teaches at least one apparatus for loading a second output bit map including a combination of output data rails and time slots from the first output bit map, where the second output bit map is configurable for being loaded in parallel with the first output bit map.

Lindberg, on the other hand, teaches that a multiplexer determines the speech store in a speech store column from which data should be read in response to control information stored in an associated control store. In particular, Lindberg teaches that the selected data from the speech stores is transmitted from the multiplexer to associated output lines referred to as Highway Vertical HWVs. As such, Lindberg merely teaches the use of a control store and

an associated multiplexer for transmitting information from a speech store to an associated output line.

Furthermore, in the Office Action, the Examiner asserts that the first input bit map of Applicants' claim 7 and second output bit map of Applicants' claim 8 are taught by Lindberg's matrix of speech stores. The matrix of speech stores taught in Lindberg, however, merely comprises memory for storing input data. The data stored in the speech stores is merely stored data, not output data. In other words, the data stored in the speech stores is not output data until the data has been selected from the speech stores for transmission over the Highway Vertical HWVs output line via the multiplexer associated with that column of the speech store. As such, the matrix of speech stores, as taught in Lindberg, simply cannot comprise an output bit map, as taught in Applicants' invention of at least claim 1.

Moreover, nowhere in Lindberg is there any teaching or suggestion of a first output bit map and a second output bit map, as taught in the Applicants' invention of at least claim 1. As such, Lindberg fails to teach or suggest each and every element of Applicants' invention of claim 1. Therefore, the Applicants submit that independent claim 1 is not anticipated by Lindberg and, as such, fully satisfies the requirements of 35 U.S.C. §102 and is patentable thereunder.

Furthermore, independent claims 5, 6, 11, and 16 include features substantially similar to the relevant features of claim 1. In particular, independent claims 5, 6, and 16 include limitations associated with first and second output bit maps that are substantially similar to the corresponding first and second output bit map limitations of claim 1. Similarly, independent claim 11 includes limitations for first and second input bit maps that are substantially related to the first and second output bit map limitations of independent claims 1, 5, 6, and 16. Just as Lindberg is completely devoid of any teaching or suggestion of first and second output bit maps, Lindberg is completely devoid of any teaching or suggestion of first and second input bit maps. As such, Lindberg does not teach or suggest each and every element of independent claims 5, 6, 11, and 16. Therefore,

claims 5, 6, 11, and 16 are not anticipated by Lindberg and, as such, fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder.

As such, Applicants submit that independent claims 1, 5, 6, 11, and 16 are not anticipated by Lindberg. Furthermore, dependent claims 2-4, 9-10, 15, and 17 depend directly or indirectly from independent claims 1, 5, 6, 11, and 16 and recite additional limitations thereof. As such, and for at least the same reasons discussed above with respect to independent claims 1, 5, 6, 11, and 16, Applicants submit that these dependent claims are also not anticipated by Lindberg and are allowable under 35 U.S.C. §102. Therefore, Applicants respectfully request that the rejections be withdrawn.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. § 102. Therefore, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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